comparison logic for comparing the digital values with limit values to generate flag values, wherein the flag values are stored in predefined locations within the memory during operation of the optoelectronic transceiver.

2. The single-chip integrated circuit of claim 1, further including:

a cumulative clock for generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable via the interface.

3. The single-chip integrated circuit of claim 1, further including:

a cumulative clock for generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is stored comprises one of the memory arrays of the memory.

4. The single-chip integrated circuit of claim 1, further including:

a power supply voltage sensor coupled to the analog to digital conversion circuitry, the power supply voltage sensor generating a power level signal corresponding to a power supply voltage level of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory.

5. The single-chip integrated circuit of claim 4, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

6. The single-chip integrated circuit of claim 5, wherein

the comparison logic includes logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the

digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory; and

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

7. The single-chip integrated circuit of claim 4, wherein

the comparison logic includes logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

8. The single-chip integrated circuit of claim 1, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

9. The single-chip integrated circuit of claim 8, wherein

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

10. The single-chip integrated circuit of claim 1, further including

fault handling logic, coupled to the transceiver for receiving at least one fault signal from the transceiver, coupled to the memory to receive at least one flag value stored in the memory, and coupled to a host interface to transmit a computed fault signal, the fault handling logic including computational logic for logically combining the at least one fault

signal received from the transceiver and the at least one flag value received from the memory to generate the computed fault signal.

11. The single-chip integrated circuit of claim 1, further including

control adjustment circuitry for adjusting a first control signal of the control signals generated by the control circuitry in accordance with an adjustment value stored in the memory.

12. The single-chip integrated circuit of claim 1, wherein the control circuitry generates the first control signal in accordance with a temperature.

13. The single-chip integrated circuit of claim 1, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

14. (Twice Amended) A single-chip integrated circuit for monitoring an optoelectronic device, comprising:

memory, including one or more memory arrays for storing information related to the optoelectronic device;

analog to digital conversion circuitry for receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory; and

a memory interface for allowing a host to read directly from and write directly to locations within the memory in accordance with commands received from a host device.

15. The single-chip integrated circuit of claim 14, further including:

a cumulative clock for generating a time value corresponding to cumulative operation time of the optoelectronic device, wherein the generated time value is readable via the memory interface.

16. The single-chip integrated circuit of claim 14, further including:

a cumulative clock for generating and storing in a register a time value corresponding to cumulative operation time of the optoelectronic device, wherein the register in which the time value is stored comprises one of the memory arrays of the memory.

17. The single-chip integrated circuit of claim 14, further including:

a power supply voltage sensor coupled to the analog to digital conversion circuitry, the power supply voltage sensor generating a power level signal corresponding to a power supply voltage level of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory.

18. The single-chip integrated circuit of claim 17, further including:

comparison logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

19. The single-chip integrated circuit of claim 18, further including

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

20. The single-chip integrated circuit of claim 19, wherein

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

21. The single-chip integrated circuit of claim 14, further including

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

22. The single-chip integrated circuit of claim 21, further including

comparison logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

23. The single-chip integrated circuit of claim 14, further including

fault handling logic, coupled to the optoelectronic device for receiving at least one fault signal from the optoelectronic device, coupled to the memory to receive at least one flag value stored in the memory, and coupled to a host interface to transmit a computed fault signal, the fault handling logic including computational logic for logically combining the at least one fault signal received from the optoelectronic device and the at least one flag value received from the memory to generate the computed fault signal.

24. The single-chip integrated circuit of claim 14, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

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25. (Amended) A single-chip integrated circuit for controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

analog to digital conversion circuitry for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined memory mapped locations within the integrated circuit;

comparison logic for comparing the digital values with limit values to generate flag values, wherein the flag values are stored in predefined memory mapped locations within the integrated circuit during operation of the optoelectronic transceiver;

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the integrated circuit; and

a memory mapped interface for allowing a host to read directly from and write directly to locations within the integrated circuit and for accessing memory mapped locations within the integrated circuit for controlling operation of the control circuitry.

26. (Amended) A method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

in accordance with instructions received from a host device, enabling the host device to read directly from and write directly to locations within a memory; and

receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined locations within the memory during operation of the optoelectronic transceiver;

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory.

27. (Amended) The method of claim 26, further including:

generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable by the host device via a memory interface.

28. The method of claim 26, further including:

generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is accessed by the reading step as a location in the memory.

29. The method of claim 26, further including:

converting an analog power supply voltage level signal, corresponding to a voltage level of the transceiver, into a digital power level value and storing the digital power level value in a predefined power level location within the memory.

30. The method of claim 29, further including:

generating a temperature signal corresponding to a temperature of the transceiver, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

31. The method of claim 30, including

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory; and

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

32. The method integrated circuit of claim 29, including

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

33. The method of claim 26, further including:

generating a temperature signal corresponding to a temperature of the transceiver, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

34. The method of claim 33, including:

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

35. The method of 26, further including

receiving at least one fault signal from the transceiver, receiving at least one flag value stored in the memory, logically combining the at least one fault signal received from the transceiver and the at least one flag value received from the memory to generate a computed fault signal, and transmitting the computed fault signal to the host device.

36. The method of claim 26, further including

adjusting a first control signal of the control signals in accordance with an adjustment value stored in the memory.

37. The method of claim 26, wherein the method is performed by a single-chip controller integrated circuit.

38. The method of claim 26, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

39. A method of monitoring an optoelectronic device, comprising:

in accordance with instructions received from a host device, enabling the host device to read directly from and write directly to locations within a memory; and

receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

wherein the method is performed by a single-chip controller integrated circuit.

40. The method of claim 39, further including:

generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable by the host device via the memory interface.

41. The method of claim 39, further including:

generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is accessed by the reading step as a location in the memory.

42. The method of claim 39, further including:

generating a power level signal corresponding to a power supply voltage level of the optoelectronic device, converting the power level signal into a digital power level value and storing the digital power level value in a predefined power level location within the memory.

43. The method of claim 39, further including:

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

44. The method of claim 43, further including

generating a temperature signal corresponding to a temperature of the optoelectronic device, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

45. The method of claim 44, wherein

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

46. The method of claim 39, further including

generating a temperature signal corresponding to a temperature of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

47. The method of claim 46, further including

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

48. The method of claim 39, further including

receiving at least one fault signal from the optoelectronic device, receiving at least one flag value stored in the memory, logically combining the at least one fault signal received from the optoelectronic device and the at least one flag value received from the memory to generate a computed fault signal, and transmit the computed fault signal to the host device.

49. The method of claim 39, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

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50. (Amended) A method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

in accordance with instructions received from a host device, enabling the host device to read directly from and write directly to locations within a controller of the optoelectronic transceiver;

receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined memory mapped locations within the controller;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined memory mapped locations within the controller during operation of the optoelectronic transceiver; and

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in the predefined memory mapped locations within the controller.

51. The method of claim 50, further including:

generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is accessed by the reading step as a memory mapped within the controller.

52. (Amended) A single-chip integrated circuit for monitoring an optoelectronic device, comprising:

memory, including one or more memory arrays for storing information related to the optoelectronic device;

analog to digital conversion circuitry configured to receive a plurality of analog signals, the analog signals corresponding to operating conditions of the optoelectronic device, converting at least one of the received analog signals into at least one digital value, and storing the at least one digital value in at least one predefined location within the memory; and

a memory interface for allowing a host device to read directly from and write directly to locations within the memory in accordance with commands received from a host device.

53. The single-chip integrated circuit of claim 52, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in the at least one predefined location within the memory.

54. The single-chip integrated circuit of claim 52, wherein the analog to digital conversion circuitry is configured to receive a voltage signal from a source external to the single-chip integrated circuit, wherein the analog to digital conversion circuitry is configured to convert the voltage signal into a digital voltage value and to store the digital voltage value in the at least one predefined location within the memory.

55. (Amended) A single-chip integrated circuit for monitoring an optoelectronic device, comprising:

memory, including one or more memory arrays for storing information related to the optoelectronic device;

analog to digital conversion circuitry for receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic device, converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one predefined location within the memory; and

a memory interface for allowing a host device to read directly from and write directly to locations within the memory in accordance with commands received from a host device.

56. The single-chip integrated circuit of claim 55, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in the at least one predefined location within the memory.

57. The single-chip integrated circuit of claim 55, further including control circuitry, responsive to the digital temperature digital value for controlling operation of the optoelectronic device.

58. The single-chip integrated circuit of claim 55, wherein the analog to digital conversion circuitry is configured to receive a voltage signal from a source external to the single-chip integrated circuit, wherein the analog to digital conversion circuitry is configured

to convert the voltage signal into a digital voltage value and to store the digital voltage value in the at least one predefined location within the memory.

59. The single-chip integrated circuit of claim 55, further including control circuitry, responsive to the at least one digital value for controlling operation of the optoelectronic device.

60. (Amended) A method of monitoring an optoelectronic device, comprising:

storing, in one or more memory arrays, information related to the optoelectronic device;

receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic device;

converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one predefined location within the memory; and

reading directly from and writing directly to locations within the memory in accordance with commands received from a host device.

61. The method of claim 60, further including:

generating a temperature signal corresponding to a temperature of the transceiver;

the converting and storing steps including converting the temperature signal into a digital temperature value, and storing the digital temperature value in the at least one predefined location within the memory.

62. The method of claim 61, further including controlling operation of the optoelectronic device in response to the digital temperature value.

63. The method of claim 60, wherein

the receiving step includes receiving a voltage signal from a source external to the single-chip integrated circuit,

the converting and storing steps include converting the voltage signal into a digital voltage value and storing the digital voltage value in the at least one predefined location within the memory.

64. The method of claim 60, further including controlling operation of the optoelectronic device in response to the at least one digital value.

Respectfully submitted,

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